阿達特科技股份有限公司
Adapter Technology Co., Ltd.

零件規格承認書

編　號：D103-0551

料　號	83105760GR		版次	--
品　名	IC	規　格	LD5760GR(SOP-7) (SMD)(通嘉)	
廠　商	吉元亨	廠　商　料　號		

1. 樣 品 狀 態：■ 有 樣 品　□ 無 樣 品

2. 第一次使用機種 ： ATS050-P050

3. 承 認 狀 態：

□暫定承認 ， 暫定承認 _____ PCS

■正式承認 ， (1)依據承認書發行認可紀錄編號：

(2)依據暫定承認書發行之暫定號碼：

4.交 貨 時 應 注 意 事 項

Approved By	Reviewed By	Designed By	Prepared By	Issued Date
阿達特 2014.07.25 魏桂浪	阿達特 2014.07.25 魏桂浪	阿達特 2014.07.24 吳俊達	阿達特 2014.07.24 廖彥軍	阿達特科技股份有限公司 正式 研發部 發行章 阿達特-文管 2014.07.25 廖彥軍

High Voltage Green-Mode PWM Controller with BNO Function

Rev. 00

General Description

The LD5760 is a Green Mode PWM IC built-in with brown-in/ out functions in a SOP-7 or SOP-8 package. The device could therefore minimize the component counts, circuit space, and reduces the overall material cost of power applications.

The LD5760 features HV start, sleep-mode, green-mode power-saving operation, and internal slope compensation, Soft-start functions which could minimum the power loss and improve the system performance.

With complete protection with it, like OLP (Over Load Protection), OVP (Over Voltage Protection), Fast SCP (short circuit protection) and Brown-in/out protection, LD5760 prevents the circuit from being damaged under abnormal conditions.

Furthermore, the LD5760 features frequency swapping and soft driving function to minimize the noise and improve EMI.

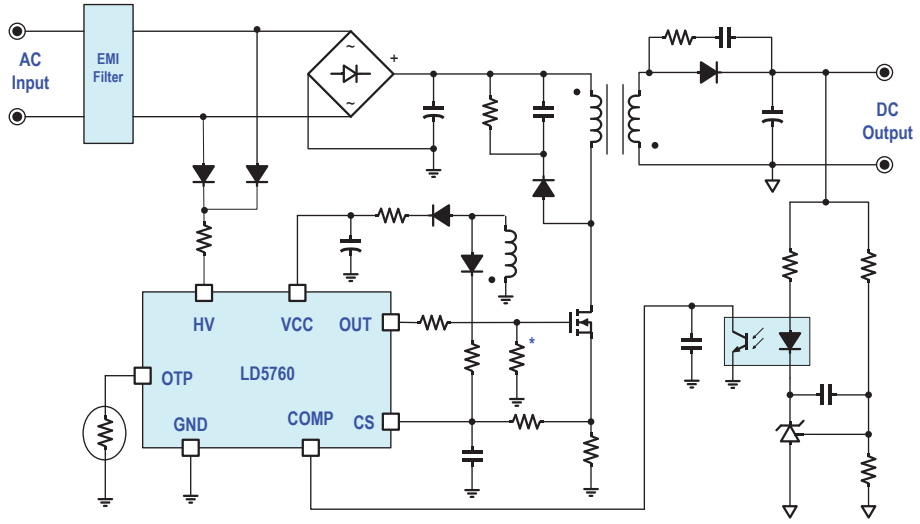
Features

- High-Voltage (500V) Startup Circuit
- Built-in Brown-in/out Function on HV pin
- Built- in X-Cap Discharge on HV pin
- Frequency Swapping for EMI improvement
- Non-Audible-Noise Green Mode Control
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- Internal OCP Compensation
- OVP (Over Voltage Protection) on Vcc/CS
- OLP (Over Load Protection)
- OTP (Over Temperature Protection)
- SCP(Short Circuit Protection)
- Soft Start
- Soft Driving
- +350mA/-800mA Driving Capability

Applications

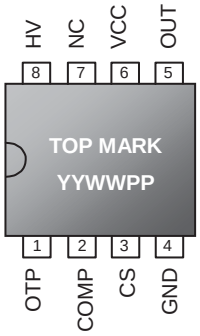
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application

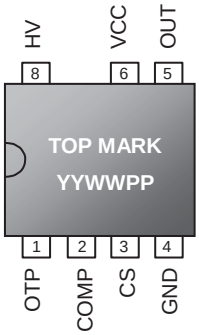


Pin Configuration

SOP-8 (TOP VIEW)



SOP-7 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

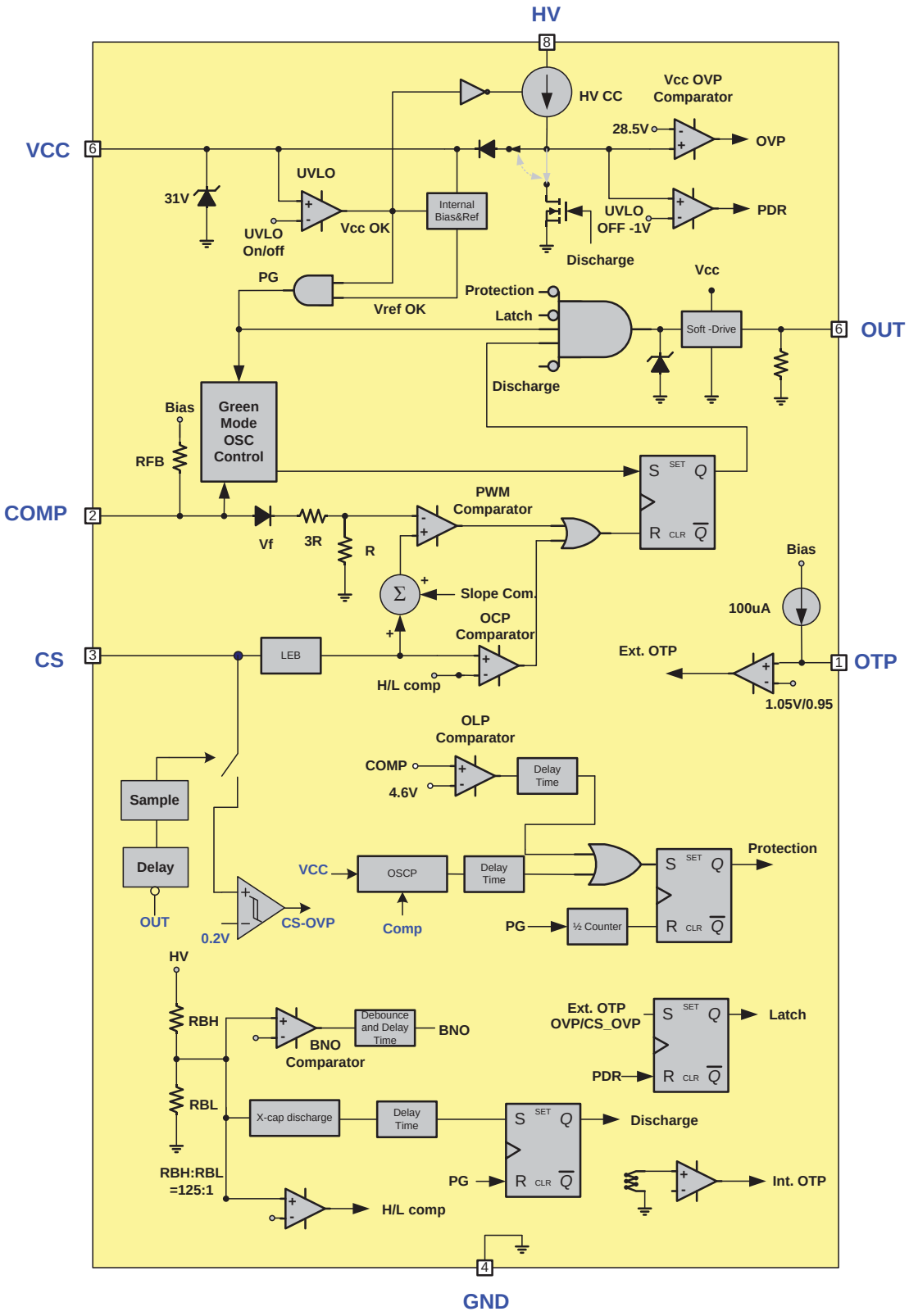
Part number	Package	Top Mark	Shipping
LD5760 GS	SOP-8	LD5760GS	2500 /tape & reel
LD5760 GR	SOP-7	LD5760GR	2500 /tape & reel

The LD5760 is RoHs compliant/ Green Packaged.

Pin Descriptions

PIN	NAME	FUNCTION
1	OTP	Pulling this pin below 0.95V will force the controller enter into latch mode and it will not resume until the AC power recycles. Connect a NTC between this pin and ground to achieve OTP protection function. Let this pin float to disable the latch protection.
2	COMP	Voltage feedback pin. Connect a photo-coupler with it to close the control loop and achieve the regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to Line/ Neutral of AC main voltage through a resistor to provide the startup current for the controller. If VCC voltage increase to trip the point of UVLO(on), this HV loop will be turned off to reduce the power loss on the startup circuit. An internal resistor divider between HV to GND pin will monitor AC line voltage to activate Brown-in/out function and sponsor with High/low line compensation to achieve constant output power limiting.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V~30V
HV	-0.3V~500V
COMP, OTP, CS	-0.3V ~6V
OUT	-0.3V ~Vcc+0.3V
Maximum Junction Temperature	150°C
Operating Ambient Temperature Range	-40°C to 85°C
Operating Junction Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8/SOP-7)	160°C/W
Power Dissipation (SOP-8/SOP-7, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except of HV Pin)	2.5KV
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model	250V
Gate Output Current	+350/-800mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Protection Mode

Part number	VCC_OVP	OSCP	CS_OVP	OLP	OTP
LD5760	Latch	Auto-Restart	Latch	Auto-Restart	Latch

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	V_{CC}< $UVLO_{(ON)}$, HV=500V	2	3	4	mA
HV Discharge capability	HV=500V	1.5	2.5	3.5	mA
HV Pin Total Input Current (HV+ BNO)	HV=500 V_{DC}, V_{CC} > $UVLO_{(ON)}$,			35	μA
HV Pin Brown-In Level (HVBI)	HV pin =half rectifier wave increase	85	95	105	V_{DC}
HV Pin Brown-out Level(HVBO)	HV pin = half rectifier wave decrease	72	80	88	V_{DC}
HV Pin BNO Hysteresis	HV_{BI}-HV_{BO}		15		V_{DC}
Brown-in De-bounce Time		100	210	300	μS
Brown-out Detection Delay time			63		mS
HV Pin Min. Operation Voltage	Vcc=15V (DetVmin = VHV-Vcc = 30V)	45			V
X-Cap discharge level	*(Fig 2.)		Peak × 77%		V
Supply Voltage (Vcc Pin)					
Startup Current	V_{CC}=15V ,HV=500V		25	50	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=3V		2.1		mA
	V_{COMP}=0V		1		mA
	Auto recover mode		0.3		mA
	Latch mode		0.47		mA
$UVLO_{OFF}$		6	7	8	V
$UVLO_{ON}$		15	16	17	V
PDR			$UVLO_{OFF}$ -1V		V
Vcc HVBI Level	HV>HVBI (Fig 1.)		$UVLO_{OFF}$ +5V		V
Vcc OVP Level		27.5	28.5	29.5	V
Vcc OVP De-bounce Time			80		μS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency					
Frequency	65KHz		65		KHz
Trembling Frequency			±8		%
Green Mode Frequency			22		KHz
Modulation Frequency			200		Hz
F_{SW} Temp. Stability	-40°C ~105°C	0	3	4	%
F_{SW} Voltage Stability	V_{CC}=8V-(OVP-1V)	0		1	%
Maximum On Time		78	83	90	%
OSCP (Output Short Circuit Protection)					
OSCP Trip Level	*		$UVLO_{OFF}$ + 3V		V
OSCP Delay Time	*Exclude soft start time.		15		ms
Voltage Feedback (Comp Pin)					
Input Voltage to Current-Sense Attenuation	*		1/4.0		V/V
Comp Impedance	V_{COMP}=3V		8		kΩ
Open Loop Voltage	COMP pin open	4.9	5.2	5.5	V
OLP Tripped Level	TC: track COMP pin open voltage		4.6		V
PWM Mode Threshold VCOMP	0.9 of F_{SW-PWM}, V_{FB_P}		2.7		V
Green Mode Threshold VCOMP	1.1 of $F_{SW-GREEN}$, V_{FB_G}		2.3		V
Zero Duty Threshold	Zero Duty, V_{FB_B}		1.9		V
VCOMP on Burst mode	Hysteresis		100		mV
Current Sensing (CS Pin)					
Maximum Input Voltage(Vcs_off)	HV=125Vdc	-3%	0.7	+3%	V
Minimum Input Voltage(Vcs_min)	HV=375Vdc	-3%	0.58	+3%	V
Leading Edge Blanking Time			250		nS
Delay to Output			70		nS
Slope Compensation Level	*0%-85% Linearly	0		0.2	V
Slope Compensation Position	*0%-85% Linearly	0		85	%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVP CS Pin					
OVP Trip Current Level		0.18	0.2	0.22	V
De-bounce Cycle			160		μS
Sample Delay Time	*		1.5		μS
Sample Time	*		1		μS
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA	0	-	1	V
Output High Level	VCC=15V, Io=20mA	9	-	Vcc	V
Rising Time	Load Capacitance= 1000pF	-	50		nS
Falling Time	Load Capacitance= 1000pF	-	20		nS
OUT Pin Clamping Voltage	V_{CC}= 21V,1nF on OUT pin		13		V
Source capability	*Load Capacitance= 33nF@out=4V		350		mA
Sink capability	*Load Capacitance=33nF		800		mA
OLP (Over Load Protection)					
OLP Delay Time	Auto restart, F_{SW}=65KHz	-10%	63	+10%	mS
Soft Start					
Soft Start Duration	*soon as OLP, OTP, BNO, OVP is tripped		6		mS
Internal OTP					
OTP Tripped Level(T_{OTP})	*		150		°C
OTP Hysteresis	*		T_{OTP}-30		°C
OTP De-bounce Time	*		160		μS
Over Temperature Protection(OTP Pin)					
OTP Pin Source Current		92	100	108	μA
Turn-On Trip Level		1.00	1.05	1.10	V
Turn-Off Trip Level		0.9	0.95	1.0	V
OTP pin de-bounce time			170		μs

*: guaranteed by design

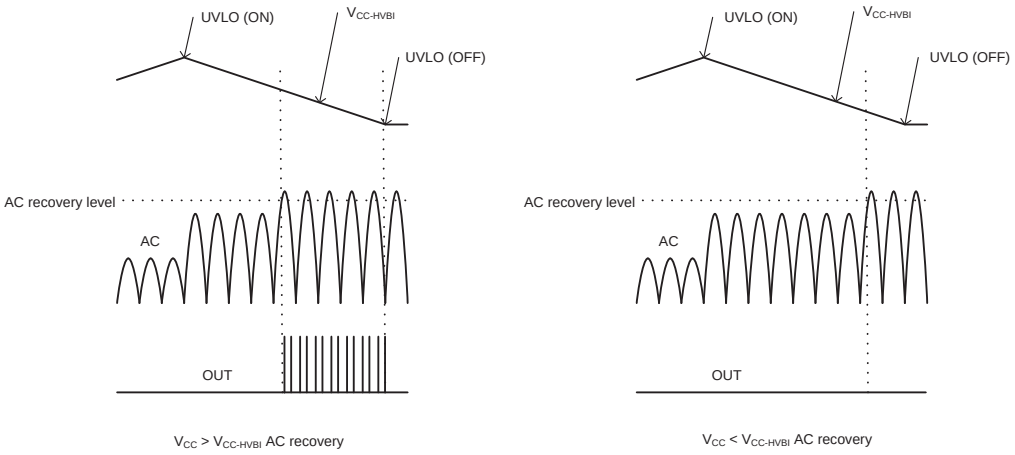


Fig 1 $V_{CC-HVBI}$ & AC recovery

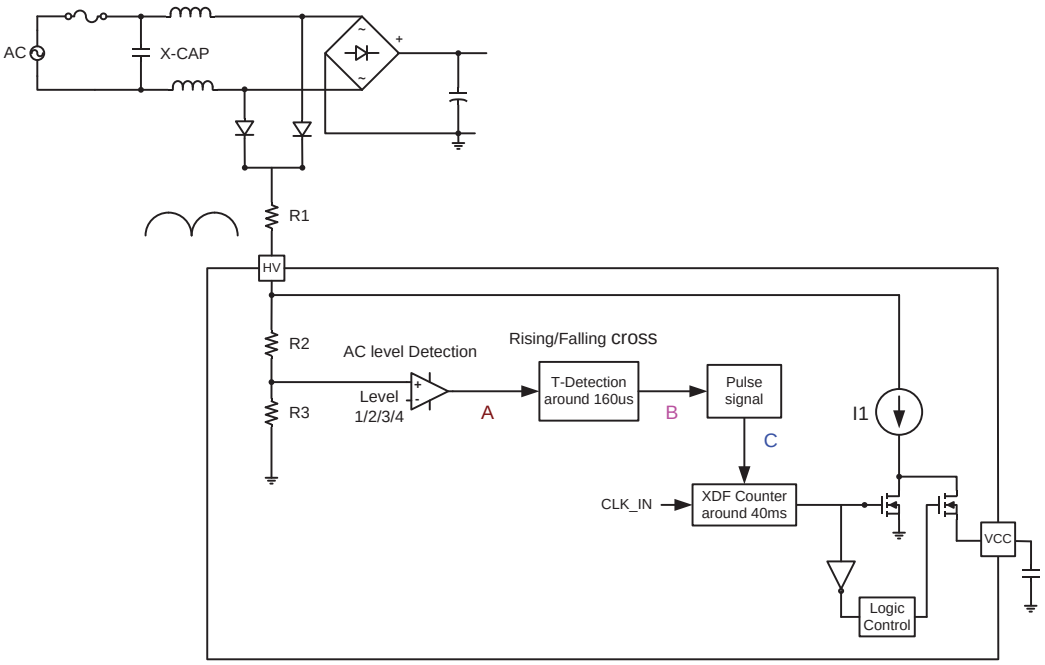


Fig. 2 X-Cap discharge Operation

Typical Performance Characteristics

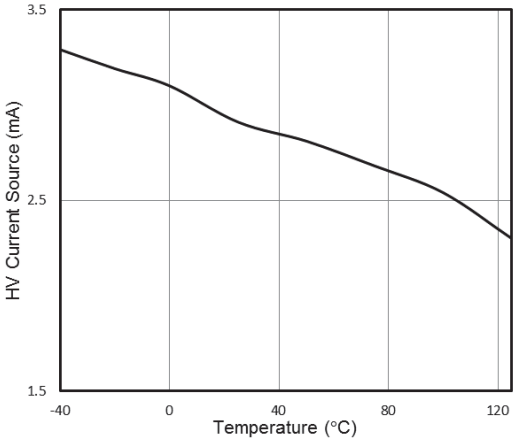


Fig.3 IHV vs. Temperature (HV=500V, Vcc=15V)

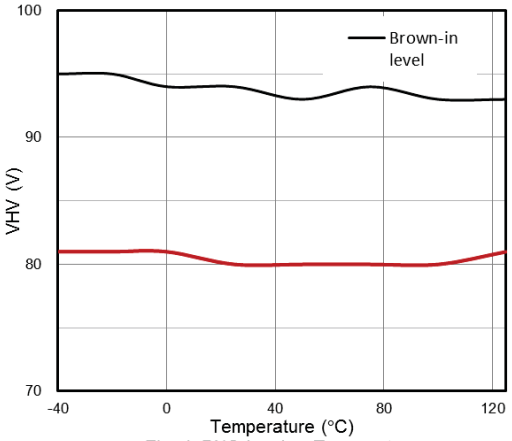


Fig. 4 BNO level vs.Temperature

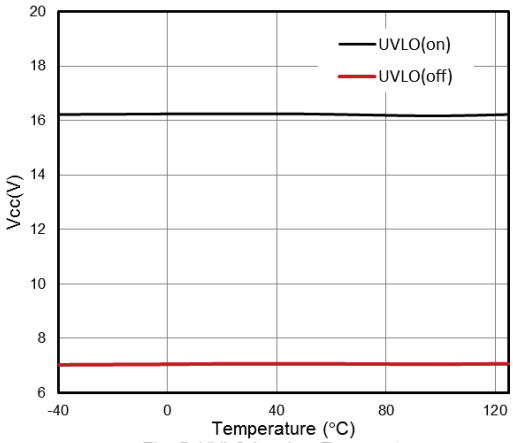


Fig. 5 UVLO level vs.Temperature

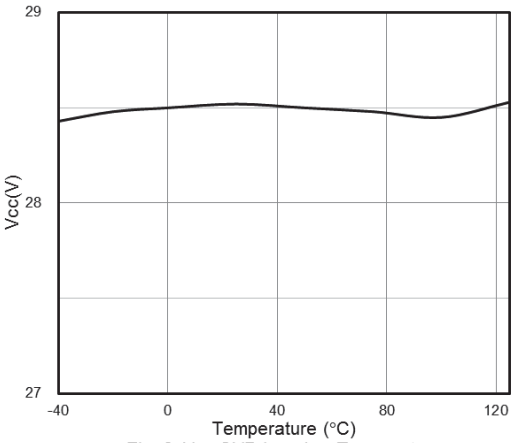


Fig. 6 Vcc OVP Level vs.Temperature

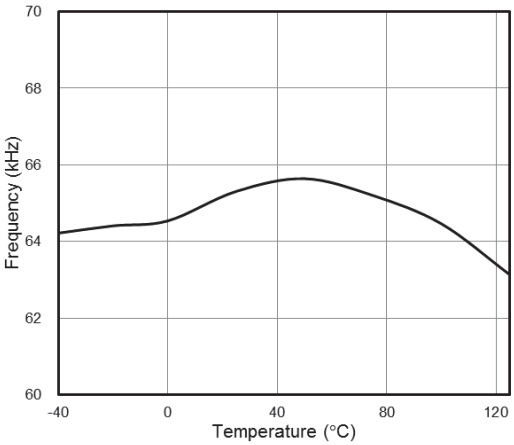


Fig. 7 Frequency vs.Temperature

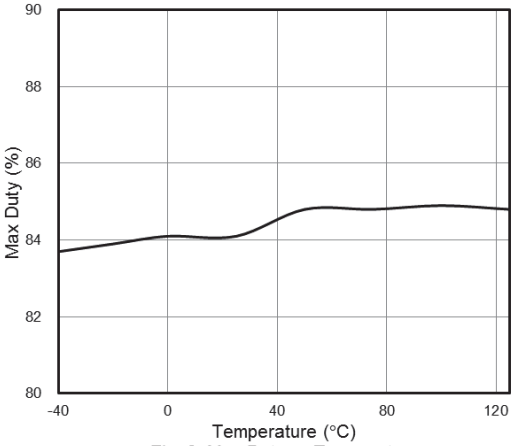


Fig. 8 Max Duty vs.Temperature

Typical Performance Characteristics

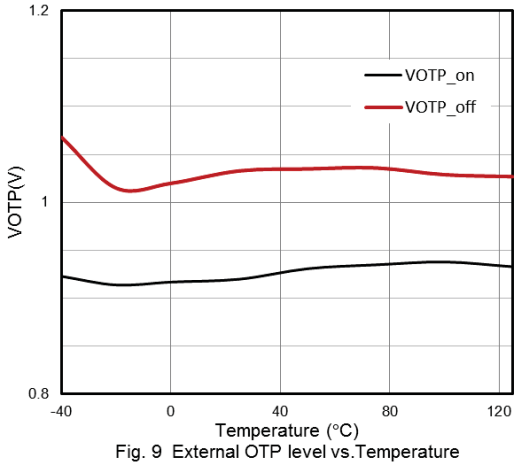


Fig. 9 External OTP level vs.Temperature

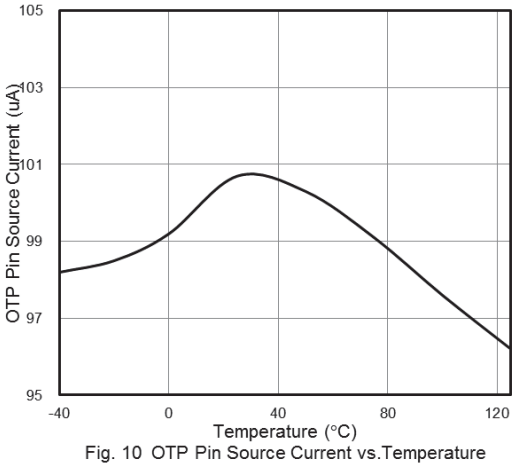


Fig. 10 OTP Pin Source Current vs.Temperature

Application Information

Operation Overview

As long as the requirement for green power becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Due to the cost and size limit, the PWM controller designer is bound to integrate with more functions to reduce the external part counts. The LD5760 is ideal for these applications. Its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes much significant power to meet the current power saving requirement. In most cases, startup resistors carry larger resistance and spend more time to start up.

To achieve the optimized topology, as shown in Fig. 11, LD5760 is implemented with a high-voltage startup circuit for such requirement. At startup, the high-voltage current source sinks current of AC Line/or Neutral to provide startup current and charge the capacitor C1 connected to VCC.

At the startup transient, the HV current will supply around 2.8mA to Vcc capacitor until this VCC voltage reaches the UVLO threshold VCC. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

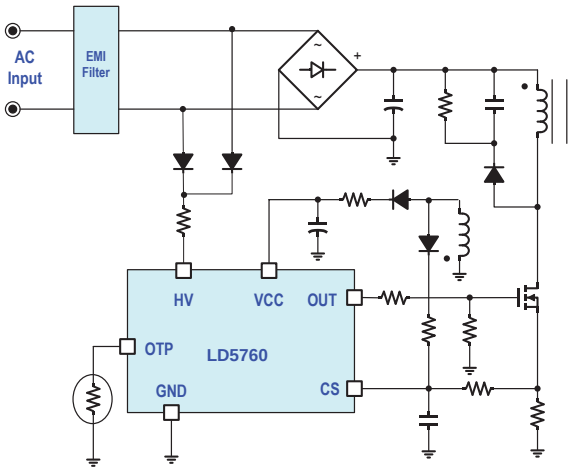


Fig. 11

As VCC trips UVLO(off), HV pin will recharge VCC capacitor till VCC voltage rises back to UVLO(on) again. Since then, HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across the Vcc pin to ensure the supply voltage enough to power on the LD5760 and in addition, to drive the power MOSFET. As shown in Fig. 12, a hysteresis is provided to prevent shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 7V, respectively.

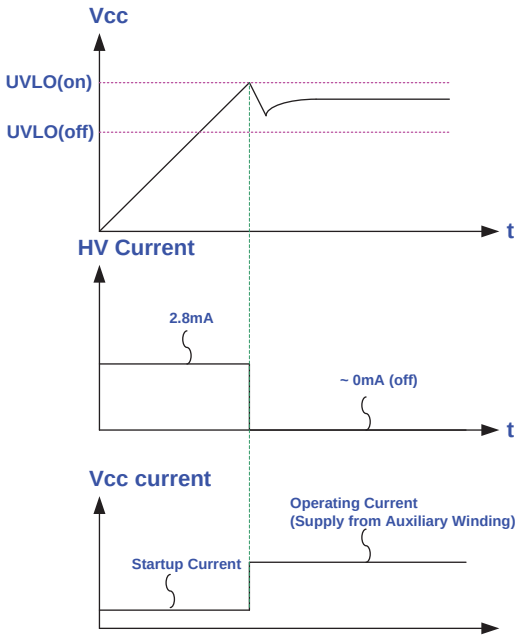


Fig. 12

Brown in/out Protection

The LD5760 features Burn-in/out function on HV pin. As the built-in comparator detects the half wave rectify line voltage condition, it will shut off the controller to prevent from any damage. Fig. 13 shows the operation. When V_{HV} < HVBO, the gate output will remain off even when the V_{CC} already reaches UVLO($_{ON}$). It therefore forces the V_{CC} hiccup between UVLO($_{ON}$) and UVLO($_{OFF}$). Unless the line voltage rises over HVBI V_{AC}, the gate output will not start switching even as the next UVLO($_{ON}$) is tripped. A hysteresis is implemented to prevent the false-triggering during turn-on and turn-off.

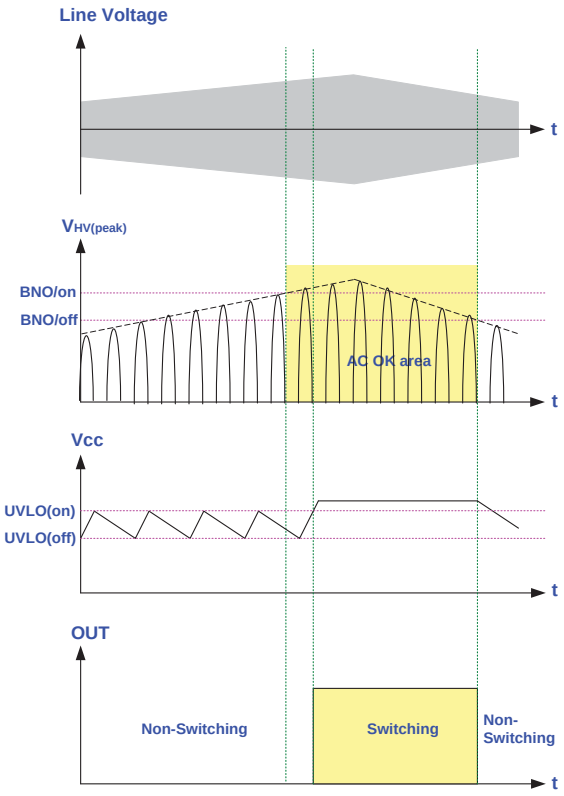


Fig. 13

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5760 detects the primary MOSFET current across CS pin to control in peak current mode and also limit the pulse-by-pulse current. The maximum voltage threshold of the current sensing pin is set at 0.7V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.7V}{R_S}$$

A 250nS leading-edge blanking (LEB) time is designed in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 150nS and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in Fig. 14) is free to eliminate.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 15) for larger power application to avoid the CS pin from being damaged by the negative turn-on spike.

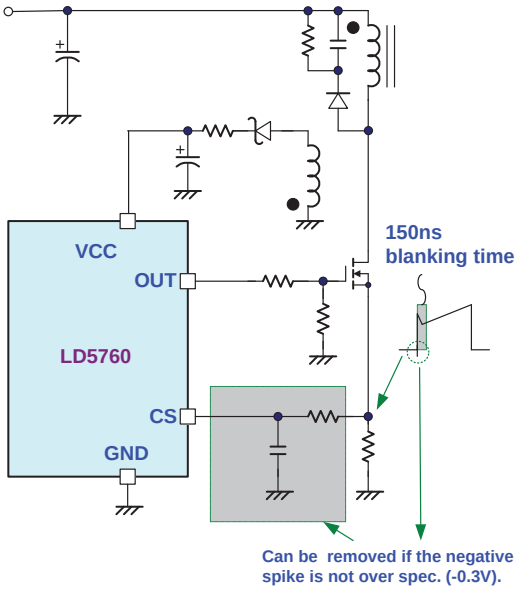


Fig. 14

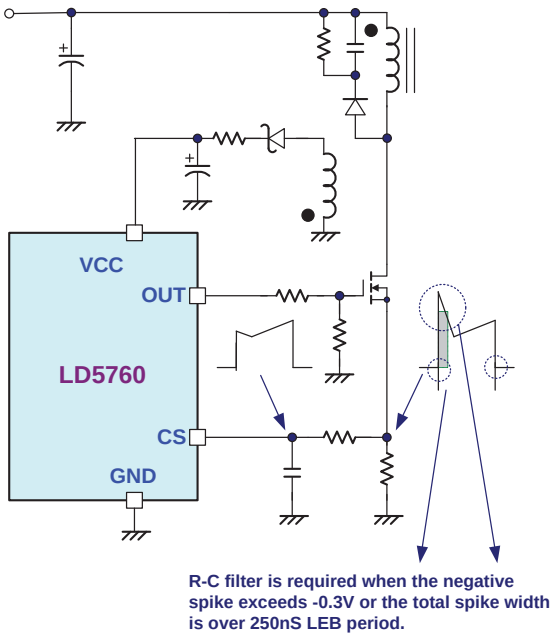


Fig. 15

Output Stage and Maximum Duty-Cycle

A CMOS buffer with output stage of typical 500mA driving capability is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5760 is limited to 83% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD5760. Similar to UC384X, its input stage is with a diode voltage offset to feed the voltage divider with 1/4 ratio, that is,

$$V_{CS(PWM\ COMPARATOR)} = \frac{1}{4} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally to optimize the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. LD5760 has internal slope compensation circuit to simplify the external circuit design.

Oscillator and Switching Frequency

The LD5760 fixes the switching frequency at 65KHz internally to optimize its performance in EMI, thermal treatment, component sizes and transformer design.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles

under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Frequency Swapping

The LD5760 is built in with frequency swapping function, which makes it easy for the power supply designers to optimize EMI performance and system cost. The trembling swapping is internally set for ±6%.

On/Off Control

Pulling COMP pin below VFB_B will immediately disable the gate output of LD5760. Remove the pull-low signal to reset it.

Over Load Protection (OLP)- Auto Recovery

To protect the circuit from being damaged during over load condition and short or open loop condition, the LD5760 is implemented with smart OLP function. LD5760 features auto recovery function of it, see Fig. 16 for the waveform. In the example of the fault condition, the feedback system will force the voltage loop enter toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP tripped level (4.6V) and stays for more than the OLP delay time, the protection will be activate and then turn off the gate output to stop the switching of power circuit. The OLP delay time is set by internal high frequency counter. It is to prevent the false triggering from the power-on and turn-off transient.

A divide-2 counter is implemented to reduce the average power under OLP behavior. As soon as OLP is activated, the output will be latched off and the divide-2 counter will start to count the number of UVLO(off). The latch will not be released until the 3rd UVLO(off) point is counted, after that the output will resume to switch again. With the protection mechanism, the average input power will be minimized, so that the component temperature and stress can be controlled within the safe operating area.

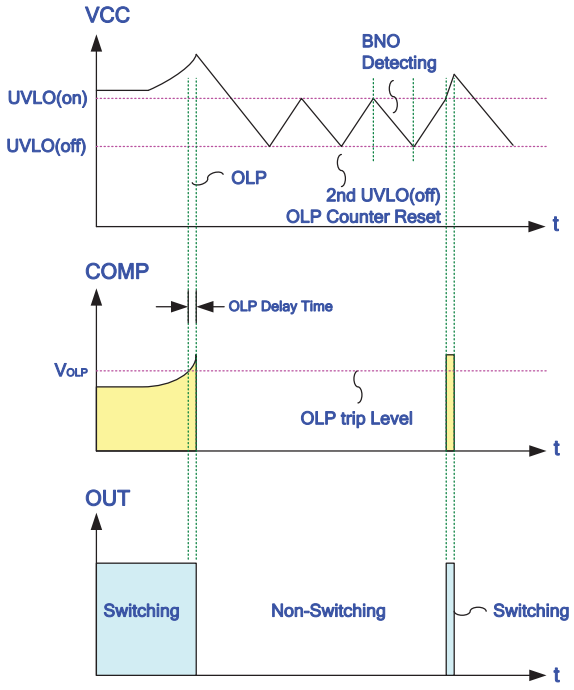


Fig. 16

OVP (Over Voltage Protection) on Vcc – Latch Mode

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 30V maximum. To protect the V_{GS} from the fault condition, LD5760 is implemented with OVP function on V_{CC}. As the V_{CC} voltage is larger than the OVP threshold voltage, the output gate drive circuit will be shut off simultaneously and stop switching the power MOSFET.

The Vcc OVP is latch-off type of protection. Once the VCC trips OVP level (which is usually caused by the feedback loop opened), it will be latched off and try to recover. Turn off AC power to let VCC fall below PDR level to release overvoltage protection. And then restart

the power to resume the operation. The de-latch level is defined by internal PDR. See Fig. 17 for its operation.

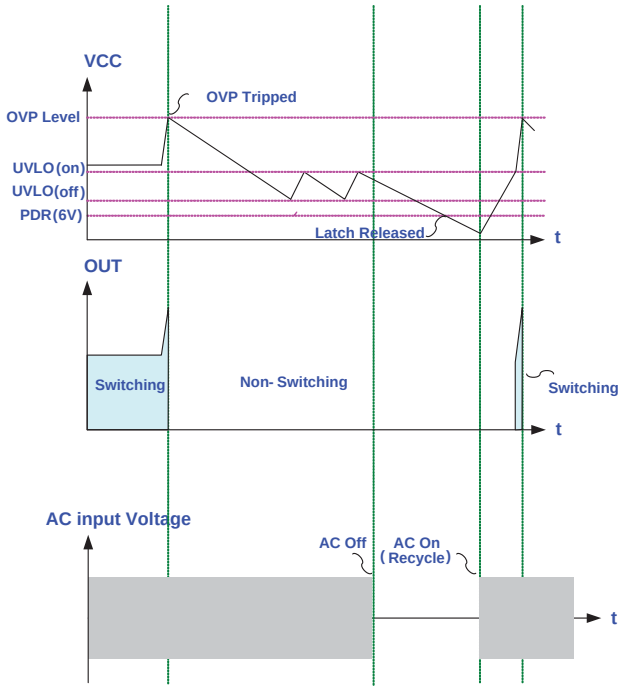


Fig. 17

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded inside the LD5760 to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

External OTP - Latched Mode Protection

The OTP circuit is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Typically, an NTC is recommended to connect with OTP pin. The NTC resistance will decrease as the device or ambient is in high temperature. The relationship is described as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

When VOTP<VOTP-off (typical1.05V), it will trigger the protection to shut down the gate output and latch off the power supply. The controller will remain latched unless the V_{CC} drops below 7V (power down reset) and V_{CC} stays on UVLO condition. Two conditions are required to restart the IC successfully, to cool down the circuit so that the NTC resistance will increase and to raise VOTP above 0.95V. Then, recycle the AC main power. The detailed operation is show in Fig. 18.

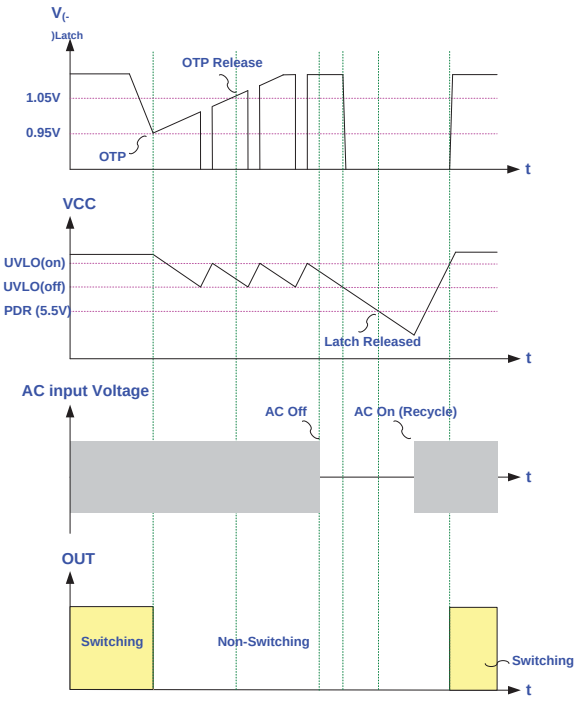


Fig. 18

Pull-Low Resistor on the Gate Pin of MOSFET

The LD5760 consists of an anti-floating resistor at OUT pin to protect the output from damage in abnormally operation or condition due to false triggering of MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig. 19, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled low and placed in

the off-state as the gate resistor is disconnected or opened in any case.

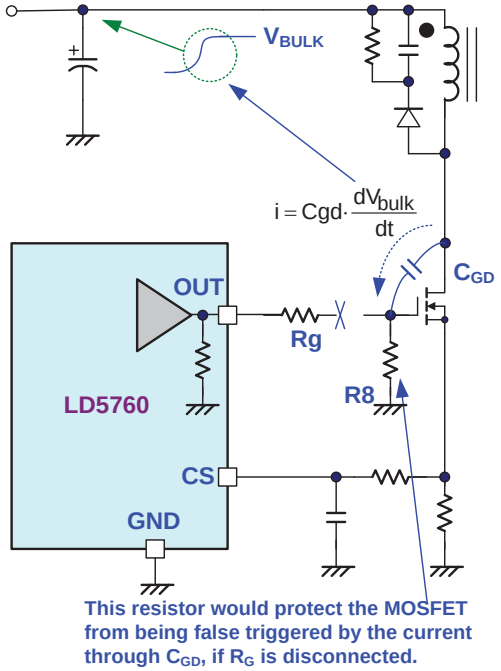


Fig. 19

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, Vcc and GND. As shown in Fig. 20, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between Vcc and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in LD5760. Fig. 21 shows the equivalent Hi-V structure circuit of LD5760. So that LD5760 is more capable to sustain negative voltage than similar products. However, a 40KΩ resistor is recommended to add in the Hi-V path to play as a current limit resistor as a negative voltage is applied.

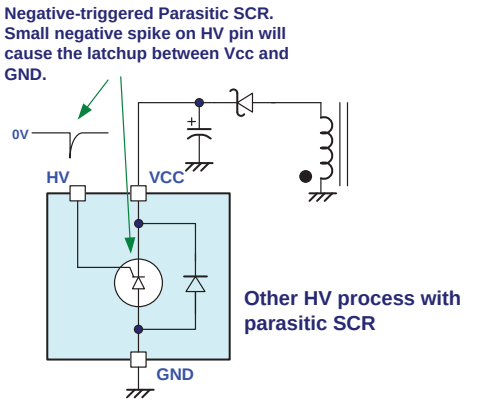


Fig. 20

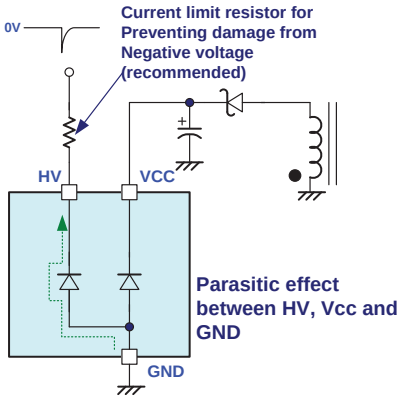
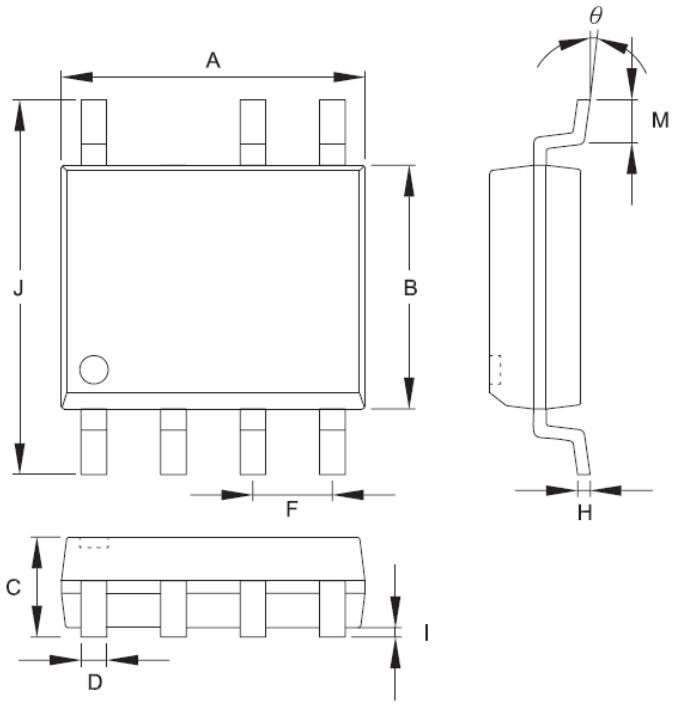


Fig. 21

Package Information

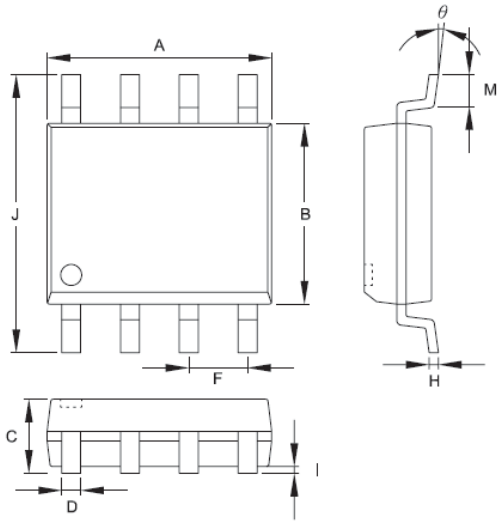
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	5/21/2013	Original Specification.