# MT8810

# **Dual N-Channel Power MOSFET**

# **General Description**

This N-channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

#### **Features**

- 20V, 7.1A R  $_{DS(on)}$ = 0.015  $\Omega$  @V  $_{GS}$  = 4.5V R  $_{DS(on)}$ = 0.017  $\Omega$  @V  $_{GS}$  = 2.5V
- Extended V<sub>GS</sub> range (±12 V) for battery applications
- HBM ESD protection level of 3.5kV typical (note 3)
- High performance trench technology for extremely low RDS(ON)
- · Low profile TSSOP-8 package

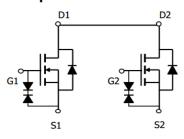
# **Applications**

- · Load switching
- · Battery charge
- · Battery disconnect circuits



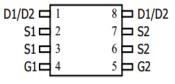
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### **Simplified Schematic**



MARKING DIAGRAM & PIN ASSIGNMENT

#### **Top View**



# **Absolute Maximum Ratings**(T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain to Source Voltage	20	V
V <sub>GS</sub>	Gate to Source Voltage	±12	V
	Drain Current Continuous ( $T_C = 25^{\circ}C$ , $V_{GS} = 4.5V$ , $R_{\theta JA} = 77^{\circ}C/W$ )	7.1	А
I <sub>D</sub>	Continuous ( $T_C = 100^{\circ}$ C, $V_{GS} = 2.5$ V, $R_{\theta JA} = 77^{\circ}$ C/W)	4.0	Α
	Pulsed	Figure 4	Α
P <sub>D</sub>	Power dissipation	1.6	W
. Б	Derate above 25°C	13	mW/°C
$T_J$ , $T_{STG}$	Operating and Storage Temperature	-55 to 150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1)	77	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	114	°C/W

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1A1H	O OOO1 O	TSSOP-8	13"	12 mm	2500 units
2					

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Flactrical	Characteristics	$T_{\Delta} = 25^{\circ}C$ unless otherwise noted
Liectifical	Cital acteriotics	$I_{\Delta} = 25^{\circ}$ C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Тур	Max	Units	
Off Characteristics								
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		20	-	-	V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16V		-	-	1	μА	
D00	Zero Gate voltage Drain Current	$V_{GS} = 0V$	T <sub>A</sub> =100°C	-	-	5	μΛ	
1	Gate to Source Leakage Current	$V_{GS} = \pm 12V$		-	-	±10	μА	
IGSS	Gate to Source Leakage Current	$V_{GS} = \pm 4.5V$				±250	nA	

#### **On Characteristics**

V <sub>GS(TH)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu A$	0.6	0.8	1.5	V
r <sub>DS(ON)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 7.1A, V <sub>GS</sub> = 4.5V	-	0.015	0.018	Ω
		I <sub>D</sub> = 6.9A, V <sub>GS</sub> = 4.0V	-	0.015	0.021	Ω
		I <sub>D</sub> = 6.5A, V <sub>GS</sub> = 3.1V	-	0.016	0.024	Ω
		I <sub>D</sub> = 6.3A, V <sub>GS</sub> = 2.5V	-	0.017	0.025	Ω

### **Dynamic Characteristics**

C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1MHz		-	1000	-	pF
C <sub>OSS</sub> C <sub>RSS</sub>	Output Capacitance			-	250	-	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			-	175	-	pF
R <sub>G</sub>	Gate Resistance	$V_{GS} = 0.5V, f = 1MH$	Z	-	2.8	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	V <sub>GS</sub> = 0V to 4.5V		-	11.5	17.3	nC
Q <sub>g(2.5)</sub>	Total Gate Charge at 2.5V		$V_{DD} = 10V$	-	7.6	11.4	nC
	Gate to Source Gate Charge		$I_D = 7.1A$ $I_0 = 1.0mA$	-	1.7	-	nC
$\frac{Q_gs}{Q_gd}$	Gate to Drain "Miller" Charge		·g	-	3.5	-	nC

# Switching Characteristics $(V_{GS} = 4.5V)$

t <sub>ON</sub>	Turn-On Time		-	-	146	ns
t <sub>d(ON)</sub>	Turn-On Delay Time	$V_{DD} = 10V, I_{D} = 7.1A$ $V_{GS} = 4.5V, R_{GS} = 6.8\Omega$	-	13	-	ns
t <sub>r</sub>	Rise Time		-	84	-	ns
t <sub>d(OFF)</sub>	Turn-Off Delay Time		-	41	-	ns
t <sub>f</sub>	Fall Time		-	55	-	ns
t <sub>OFF</sub>	Turn-Off Time		-	-	144	ns

#### **Drain-Source Diode Characteristics**

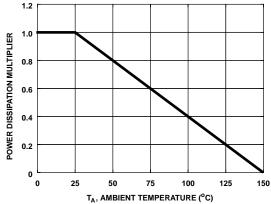
V <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = 1.3A	-	0.7	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	$I_{SD} = 7.1A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	27	ns
Q <sub>RR</sub>	Reverse Recovered Charge	$I_{SD} = 7.1A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	16	nC

2

#### Notes:

- 1.  $R_{\theta JA}$  is 77 °C/W (steady state) when mounted on a 1 inch<sup>2</sup> copper pad on FR-4.
- 2.  $\rm R_{\theta JA}\,$  is 114  $^{o}C/W$  (steady state) when mounted on a mininum copper pad on FR-4.
- 3 The diode connected to the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

# Typical Characteristic $T_A = 25^{\circ}C$ unless otherwise noted



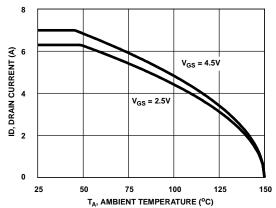


Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

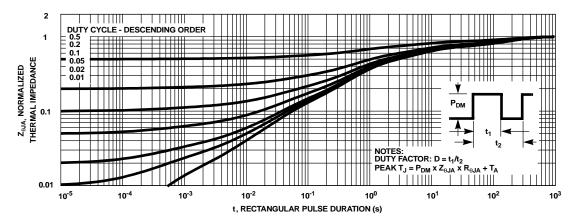


Figure 3. Normalized Maximum Transient Thermal Impedance

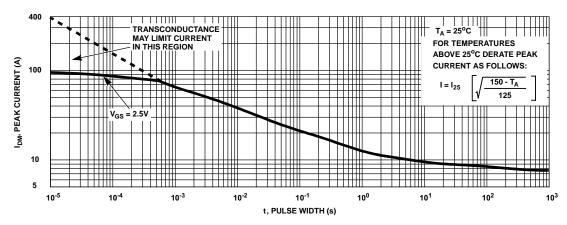
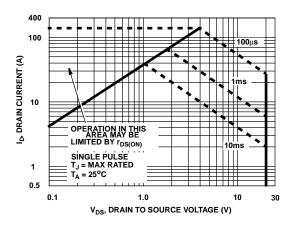


Figure 4. Peak Current Capability

3

# Typical Characteristic (Continued) T<sub>A</sub> = 25°C unless otherwise noted



40
PULSE DURATION = 80 µs
DUTY CYCLE = 0.5% MAX
VDD = 10V

T<sub>J</sub> = 150°C

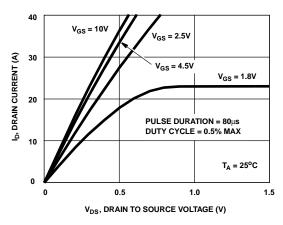
T<sub>J</sub> = 25°C

T<sub>J</sub> = -55°C

0
1.0
1.5
2.0
2.5
V<sub>GS</sub>, GATE TO SOURCE VOLTAGE (V)

Figure 5. Forward Bias Safe Operating Area

Figure 6. Transfer Characteristics



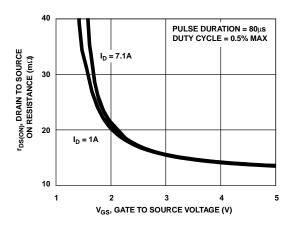
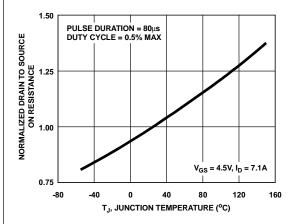


Figure 7. Saturation Characteristics

Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current



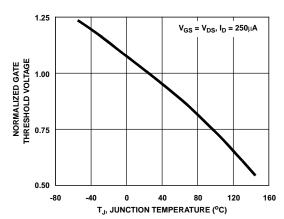
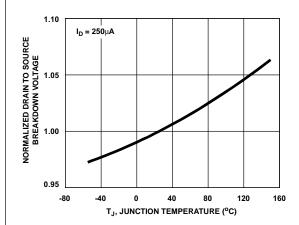


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

# Typical Characteristic (Continued) T<sub>A</sub> = 25°C unless otherwise noted



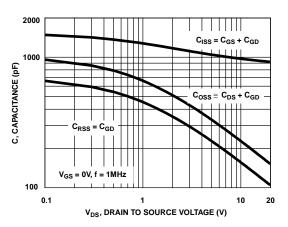


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Figure 12. Capacitance vs Drain to Source Voltage

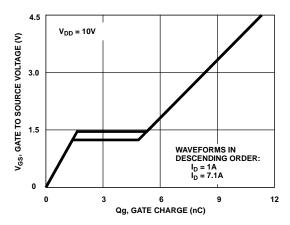


Figure 13. Gate Charge Waveforms for Constant Gate Currents

# **Test Circuits and Waveforms**

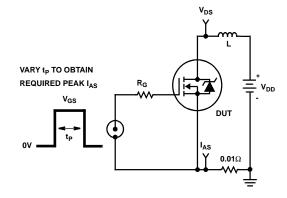


Figure 14. Unclamped Energy Test Circuit

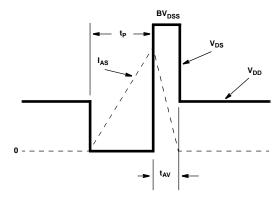


Figure 15. Unclamped Energy Waveforms

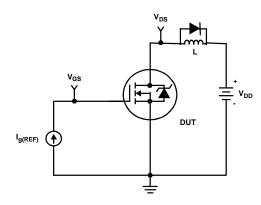


Figure 16. Gate Charge Test Circuit

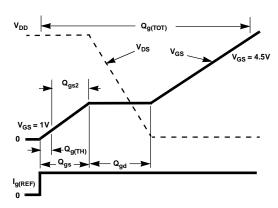


Figure 17. Gate Charge Waveforms

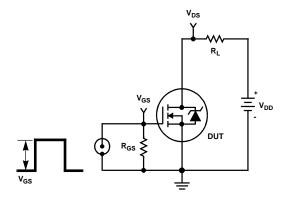


Figure 18. Switching Time Test Circuit

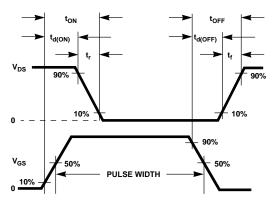
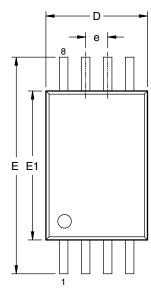
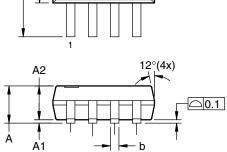


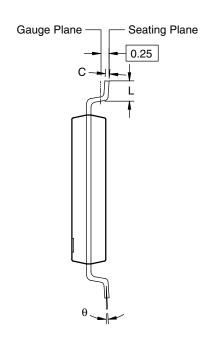
Figure 19. Switching Time Waveforms

6

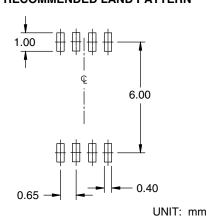
# **TSSOP-8** Package Dimensions







# RECOMMENDED LAND PATTERN



#### **Dimensions in millimeters**

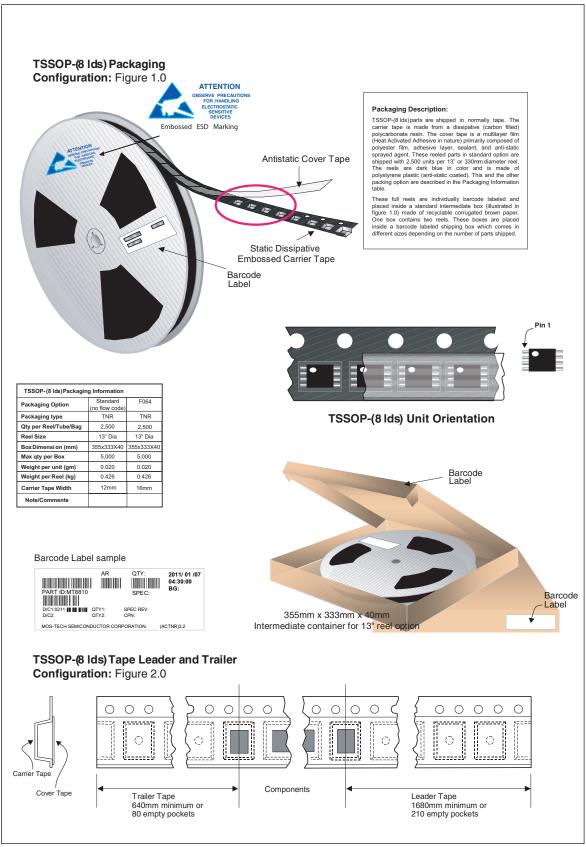
Symbols	Min.	Nom.	Max.	
Α	_	_	1.20	
A1	0.05	_	0.15	
A2	0.80	1.00	1.05	
b	0.19	_	0.30	
С	0.09	_	0.20	
D	2.90	3.00	3.10	
E	6	6.40 BSC		
E1	4.30	4.40	4.50	
е	0.65 BSC			
L	0.45	0.60	0.75	
θ	0°	_	8°	

### **Dimensions in inches**

Min.	Nom.	Max.	
		0.047	
0.002		0.006	
0.031	0.039	0.041	
0.007	_	0.012	
0.004		0.008	
0.114	0.118	0.122	
0	.252 BS	С	
0.169	0.173	0.177	
0.026 BSC			
0.018	0.024	0.030	
0°	_	8°	
		0.002 - 0.031 0.039 0.007 - 0.004 - 0.114 0.118 0.252 BS0 0.169 0.173 0.026 BS0 0.018 0.024	

#### Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions are inclusive of plating
- 3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
- 4. Dimension L is measured in gauge plane.
- 5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
- 6. Refer to JEDEC MO-153(AA).



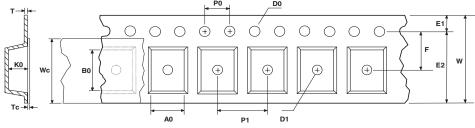
8

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# TSSOP-(8 lds) Tape and Reel Data, continued

# TSSOP-(8 Ids) Embossed Carrier Tape

Configuration: Figure 1.0



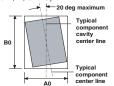
U	ser Dire	ction of F	eed	

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TSSOP-(8 lds)	6.80	3.40	12.0	1.55	1.50	1.75	10.25	5.50	8.0	4.0	1.60	0.30	9.2	0.06
(12mm)	+/-0.10	+/-0.10	+/-0.3	+/-0.05	min	+/-0.10	min	+/-0.05	+/-0.1	+/-0.1	+/-0.10	+/-0.05	+/-0.3	+/-0.02
TSSOP-(8 lds)	6.80	3.40	16 0	1.55	1.50	1.75	14.25	7.50	8.0	4.0	1.60	0.30	13.0	0.06
(16mm)	+/-0.10	+/-0.10	+/-0.3	+/-0.05	min	+/-0.10	min	+/-0.05	+/-0.1	+/-0.1	+/-0.10	+/-0.05	+/-0.3	+/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View



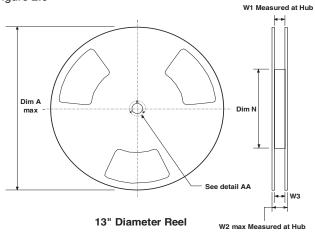
Sketch B (Top View)
Component Rotation

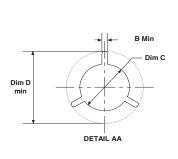


Sketch C (Top View)

#### TSSOP-(8Ids) Reel Configuration:

Figure 2.0





Dimensions are in inches and millimeters											
Tape Size	Reel Option	Dim A Dim B		Dim C	Dim D Dim N		Dim W1	Dim W2	Dim W3 (LSL-USL)		
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4		
16mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.646 + 0.078/-0.000 16.4 +2/0	0.882 22.4	0.626 - 0.764 15.9 - 19.4		

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- 8. 除上述第7项内容外,不能将本资料中记载的产品用于以下用途。如果用于以下用途而造成的损失,本公司概不负责。
  - 1) 生命维持装置。
  - 2) 植埋于人体使用的装置。
  - 3) 用于治疗(切除患部、给药等)的装置。
  - 4) 其他直接影响到人的生命的装置。
- 9. 在使用本资料所记载的产品时,对于最大额定值、工作电源电压的范围、放热特性、安装条件及其他条件请在本公司规定的保证范围内使用。如果超出了本公司规定的保证范围使用时,对于由此而造成的故障和出现的事故,本公司将不承担任何责任。
- 10. 本公司一直致力于提高产品的质量和可靠性,但一般来说,半导体产品总会以一定的概率发生故障、或者由于使用条件不同而出现错误运行等。为了避免因本公司的产品发生故障或者错误运行而导致人身事故和火灾或造成社会性的损失,希望客户能自行负责进行冗余设计、采取延烧对策及进行防止错误运行等的安全设计(包括硬件和软件两方面的设计)以及老化处理等,这是作为机器和系统的出厂保证。特别是单片机的软件,由于单独进行验证很困难,所以要求在顾客制造的最终的机器及系统上进行安全检验工作。
- 11. 如果把本资料所记载的产品从其载体设备上卸下,有可能造成婴儿误吞的危险。顾客在将本公司产品安装到顾客的设备上时,请顾客自行负责将本公司产品设置为不容易剥落的安全设计。如果从顾客的设备上剥落而造成事故时,本公司将不承担任何责任。
- 12. 在未得到本公司的事先书面认可时,不可将本资料的一部分或者全部转载或者复制。
- 13. 如果需要了解关于本资料的详细内容,或者有其他关心的问题,请向本公司的营业窗口咨询。

#### Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.