

# MT6010

## 60V N-Channel Power

### General Description

These N-Channel enhancement mode power field effect transistors are produced using Mos-tech's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

### Features

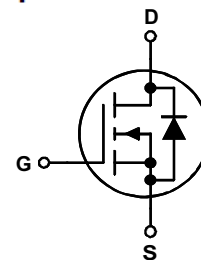
- 15A, 60V,  $R_{DS(on)} = 30m\ \Omega$  (Typ.)@  $V_{GS} = 10V$
- Low gate charge ( typical 11.5 nC)
- Low Crss ( typical 25 pF)
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability
- 175 °C maximum junction temperature rating



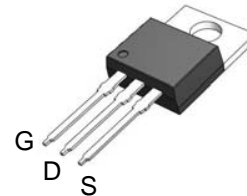
**MT Semiconductor®**

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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



TO-220FB-3L

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	MT6010	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	15	A
		10.1	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	50	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	105	mJ
$I_{AR}$	Avalanche Current (Note 1)	20	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	53	W
		0.35	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.85	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.07	--	$\text{V}^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 48\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	3.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	--	0.03	0.05	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 10\text{ A}$ (Note 4)	--	12	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	480	590	pF
$C_{oss}$	Output Capacitance		--	170	220	pF
$C_{rss}$	Reverse Transfer Capacitance		--	25	35	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 10\text{ A},$ $R_G = 25\ \Omega$	--	5	20	ns
$t_r$	Turn-On Rise Time		--	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	25	60
$Q_g$	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 10\text{ V}$	--	11.5	15	nC
$Q_{gs}$	Gate-Source Charge		--	3	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	4.5	--

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	15	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	80	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 10\text{ A},$	--	43	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	50	--	nC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 450\ \mu\text{H}, I_{AS} = 10\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 20\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

### Typical Characteristics

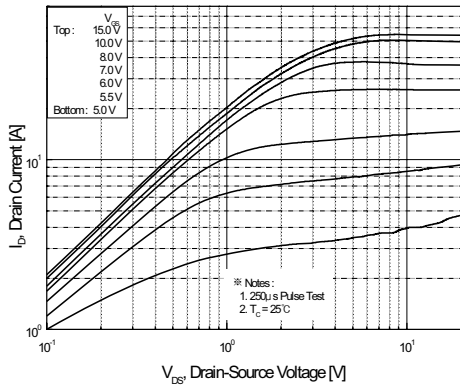


Figure 1. On-Region Characteristics

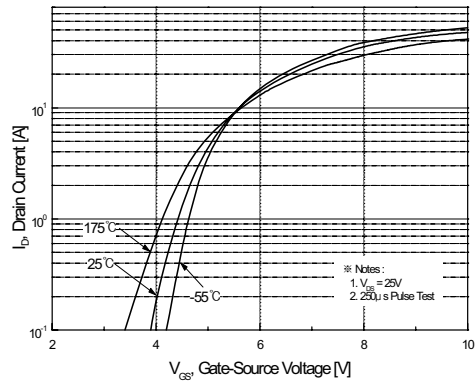


Figure 2. Transfer Characteristics

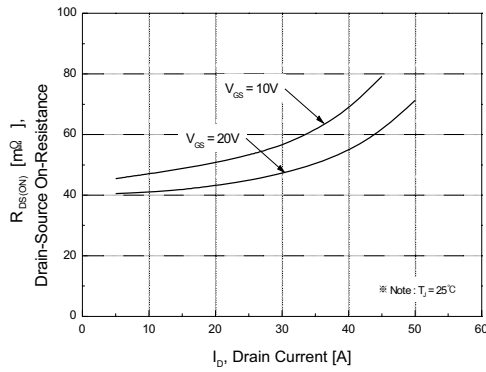


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

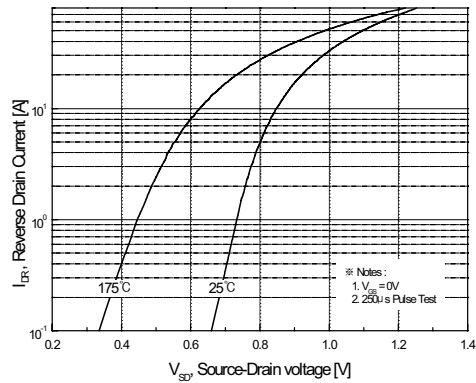


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

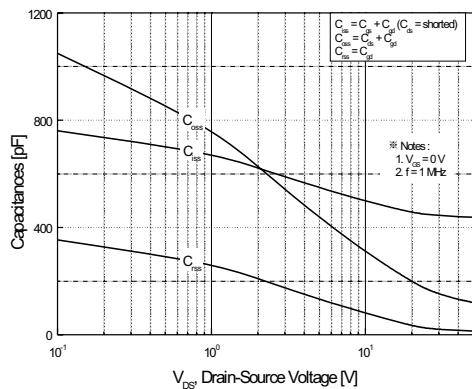


Figure 5. Capacitance Characteristics

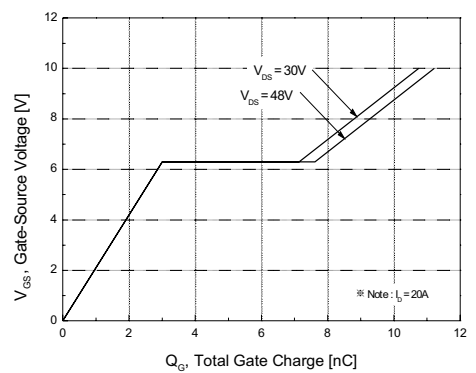


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

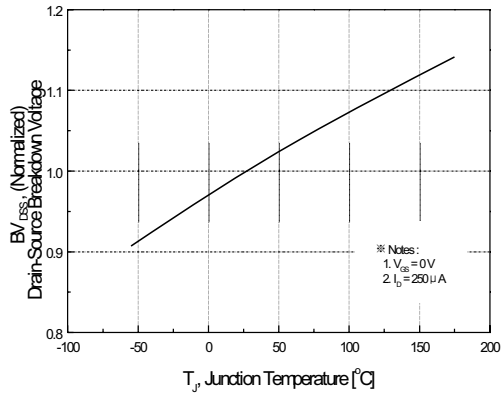


Figure 7. Breakdown Voltage Variation vs. Temperature

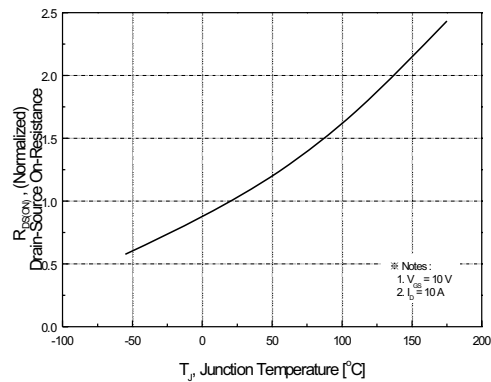


Figure 8. On-Resistance Variation vs. Temperature

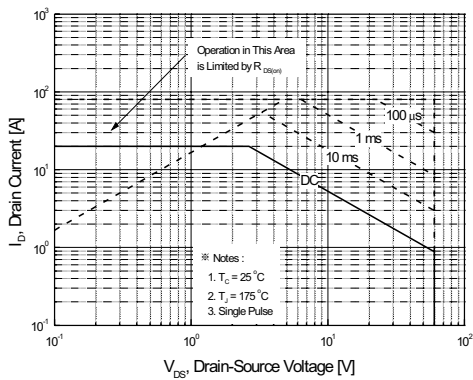


Figure 9. Maximum Safe Operating Area

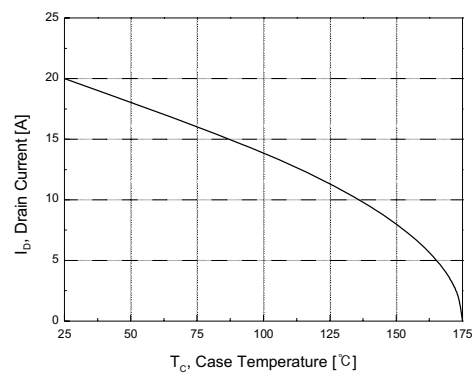


Figure 10. Maximum Drain Current vs. Case Temperature

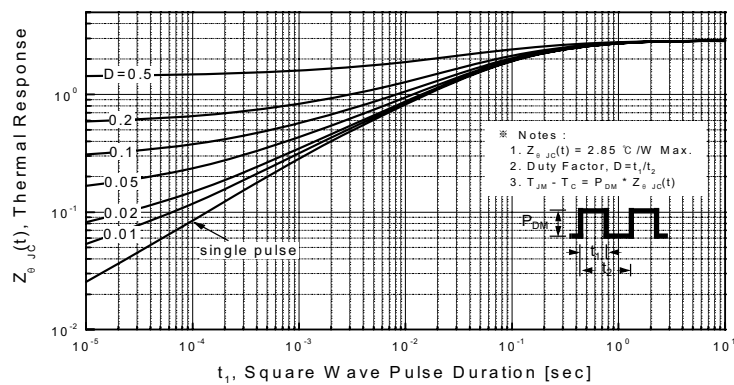
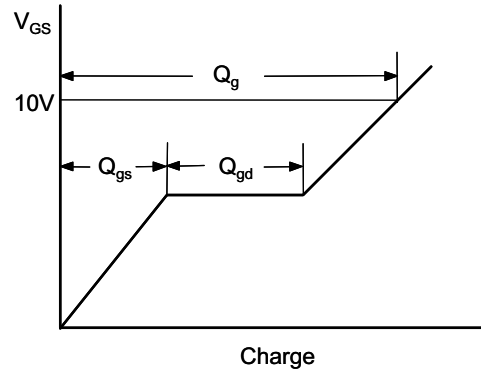
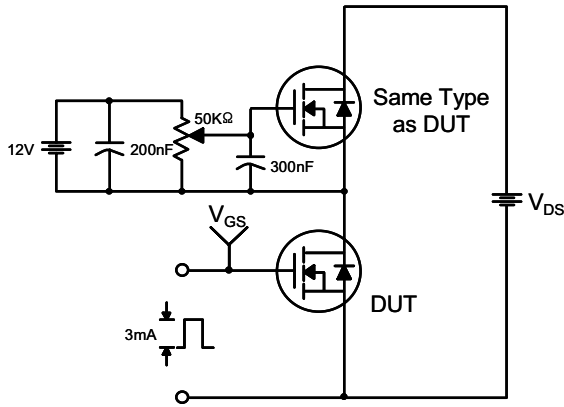
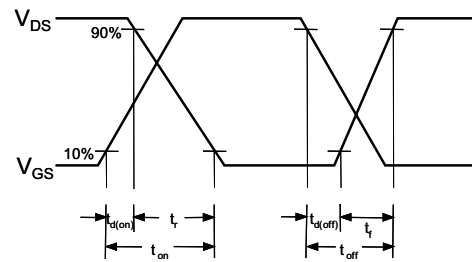
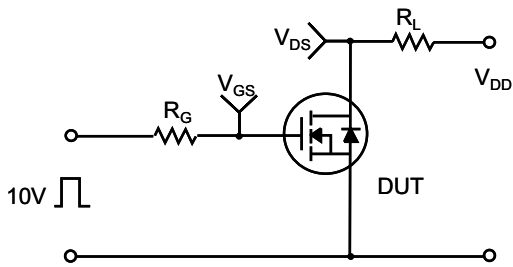


Figure 11. Transient Thermal Response Curve

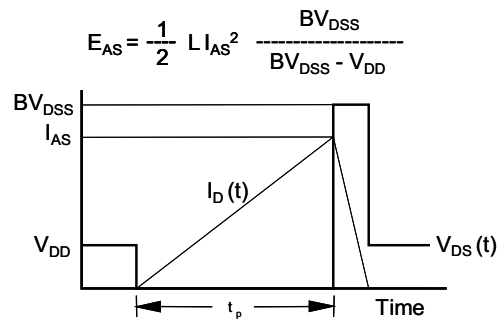
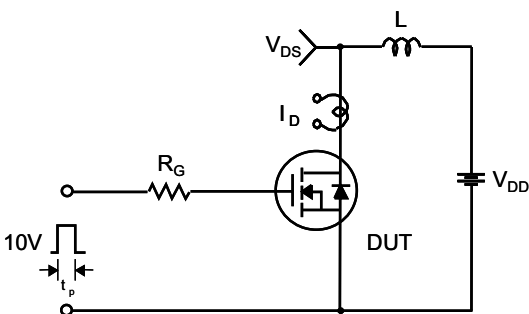
**Gate Charge Test Circuit & Waveform**



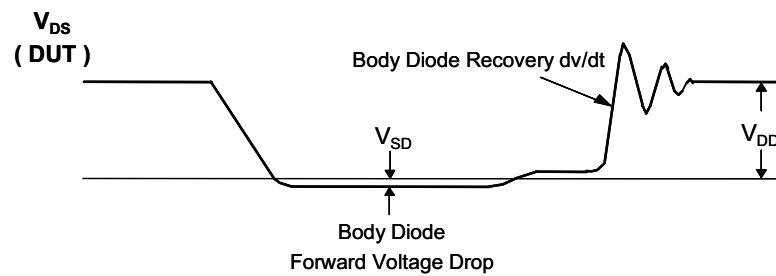
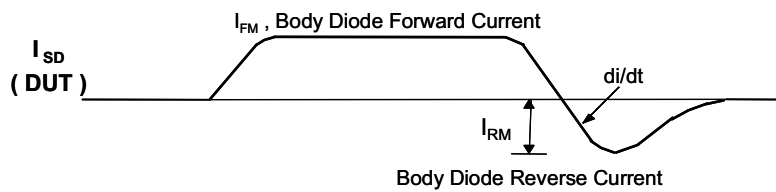
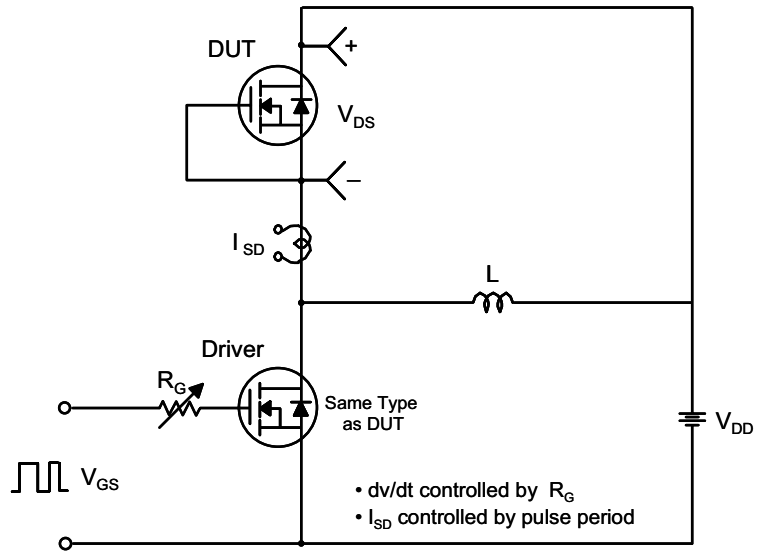
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

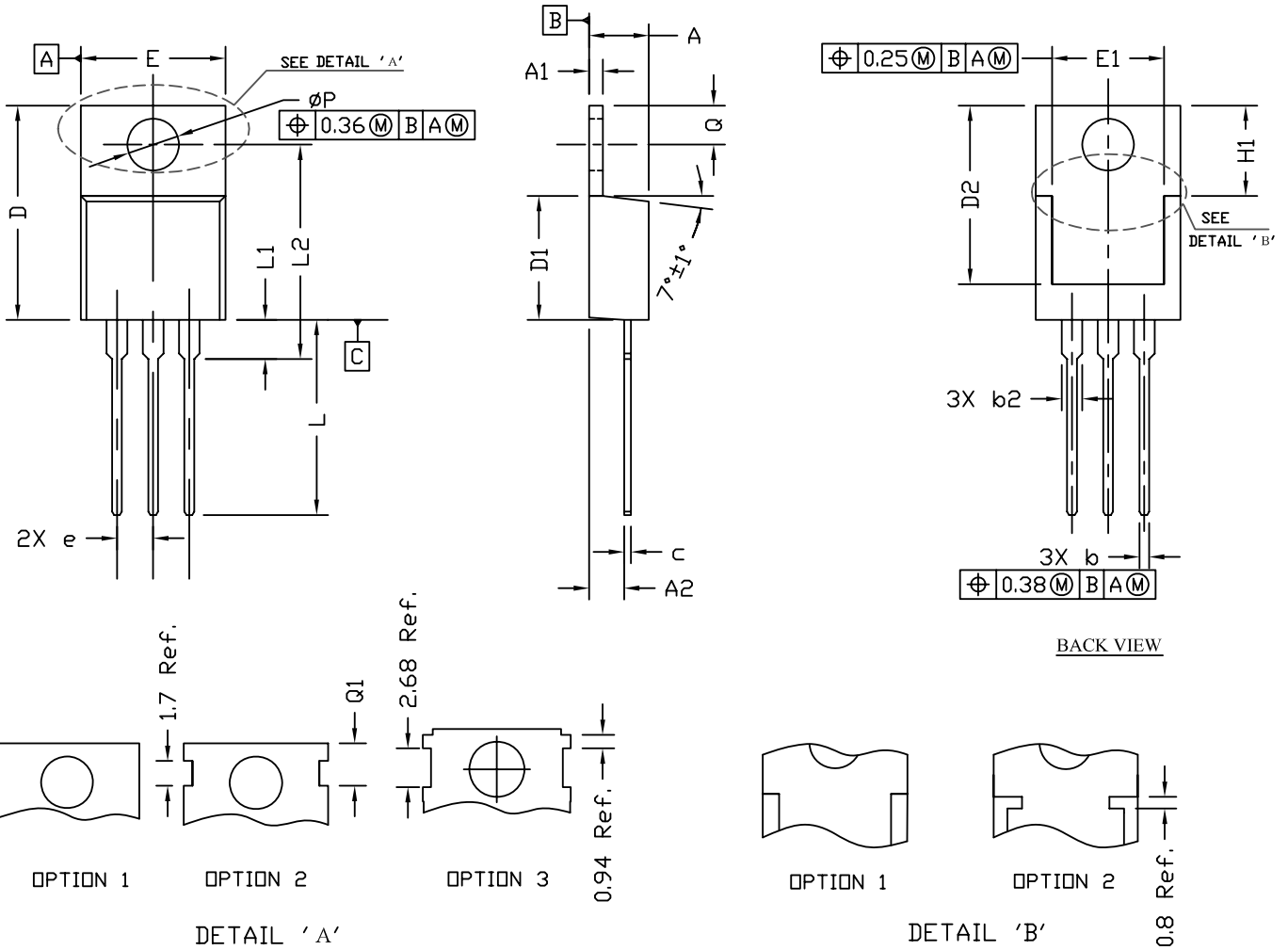


Peak Diode Recovery dv/dt Test Circuit & Waveforms

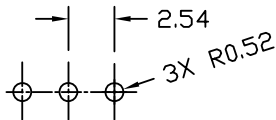


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Version	L

TO220 PACKAGE OUTLINE



RECOMMENDATION OF HOLE PATTERN



UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.45	4.72	0.169	0.175	0.186
A1	1.15	1.27	1.40	0.045	0.050	0.055
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.69	0.81	0.95	0.027	0.032	0.037
b2	1.17	1.37	1.45	0.046	0.050	0.068
c	0.36	0.38	0.60	0.014	0.015	0.024
D	14.50	15.44	15.80	0.571	0.608	0.622
D1	8.59	9.14	9.65	0.338	0.360	0.380
D2	11.43	11.73	12.48	0.450	0.462	0.491
e	2.54 BSC			0.100 BSC.		
E	9.66	10.03	10.54	0.380	0.395	0.415
E1	6.22	---	---	0.245	---	---
H1	6.10	6.30	6.50	0.240	0.248	0.256
L	12.27	12.82	14.27	0.483	0.505	0.562
L1	2.47	---	3.90	0.097	---	0.154
L2	---	---	16.70	---	---	0.657
Q	2.59	2.74	2.89	0.102	0.108	0.114
$\phi P$	3.50	3.84	3.89	0.138	0.151	0.153
Q1	2.70	---	2.90	0.106	---	0.114

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### Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.